CLAIMS:

1. A method of fabricating a semiconductor device, the method comprising:

determining a first dimension of a gate electrode structure;

choosing a target trimmed dimension;

feeding forward the first dimension and the target trimmed dimension to a process model to create a set of process parameters; and

performing a trimming process on the gate electrode structure, including:

controlling the set of process parameters in the trimming process, and

trimming the gate electrode structure.

2. The method according to claim 1, further comprising measuring a trimmed dimension of the trimmed gate electrode structure.

3. The method according to claim 2, further comprising repeating the performing at least once until the target trimmed dimension is obtained.

4. The method according to claim 3, wherein the performing further comprises feeding backward the trimmed dimension to the process model to create a new set of process parameters.

5. The method according to claim 1, wherein the creating of the set of process parameters comprises

calculating a reaction layer thickness from the first dimension, the trimmed dimension, the target trimmed dimension or a combination of two or more thereof; and

determining the set of process parameters based on the reaction layer thickness.

6. The method according to claim 5, wherein the determining further comprises selecting at least one process parameter while keeping other process parameters fixed.

7. The method according to claim 1, wherein the set of process parameters comprises process gas pressure, substrate temperature, plasma power, or process time or a combination of two or more thereof.

8. The method according to claim 1, wherein the measuring comprises using a scattering technique, a scanning electron microscope (SEM), or both to determine the first dimension.

9. The method according to claim 1, wherein the trimming comprises

forming a reaction layer through reaction with the gate electrode structure; and

selectively removing the reaction layer from the unreacted portion of the gate electrode structure by chemical etching.

10. The method according to claim 9, wherein the reaction layer is formed in a self-limiting process.

11. The method according to claim 9, wherein the forming comprises exposing the gate electrode structure to a reactant gas in a thermal process, a plasma process or both.

12. The method according to claim 11, wherein the reactant gas comprises an excited oxygen-containing gas.

13. The method according to claim 9, wherein the forming comprises exposing the gate electrode structure to a wet oxidation process.

14. The method according to claim 9, wherein the selectively removing comprises exposing the gate electrode structure to an etch gas.

15. The method according to claim 9, wherein the selectively removing comprises exposing the gate electrode structure to $HF_{(aq)}$.

16. The method according to claim 9, wherein the selectively removing comprises exposing the gate electrode structure to HF and NH_3 gases and then to a heat treatment.

17. The method according to claim 9, wherein the selectively removing comprises exposing the gate electrode structure to NF_3 and NH_3 gases in a remote plasma and then to a heat treatment.

18. The method according to claim 9, wherein the selectively removing comprises exposing the gate electrode structure to a wet process.

19. The method according to claim 9, wherein the forming and the removing are carried out in a single processing system.

20. The method according to claim 9, wherein the forming and the removing are carried out in multiple processing systems.

21. The method according to claim 9, wherein the first dimension is a lithographic dimension.

22. The method according to claim 9, wherein the forming includes forming an oxide layer on a surface of the gate electrode.

23. The method according to claim 1, wherein the gate electrode structure comprises a gate electrode layer.

24. The method according to claim 23, wherein the gate electrode layer comprises a Si-containing layer, a metal-containing layer, or both.

25. The method according to claim 24, wherein the gate electrode layer includes the Si-containing layer comprising amorphous Si, poly-Si, or SiGe or a combination of two or more thereof.

26. The method according to claim 24, wherein the gate electrode layer includes the metal-containing layer comprising a metal, a metal nitride, a metal oxide or a combination of two or more thereof.

27. The method according to claim 26, wherein metal-containing layer comprises TaN, TiN, TaSiN, Ru, or RuO_2 or a combination of two or more thereof.

28. The method according to claim 23, wherein the gate electrode structure further comprises an ARC layer.

29. The method according to claim 28, wherein the ARC layer comprises an organic ARC layer or an inorganic ARC layer.

30. The method according to claim 28, wherein the ARC layer comprises SiN.

31. The method according to claim 1, further comprising using the trimmed gate electrode structure as a mask layer for anisotropic etching.

32. A computer readable medium containing program instructions for execution on a processor, which when executed by the processor, cause a processing tool to perform the steps of claim 1.

33. A semiconductor device, comprising:
a trimmed gate electrode structure formed by the method of claim 1.

34. A processing tool, comprising:
a substrate loading chamber configured for loading and unloading a substrate with a gate electrode structure having a first dimension;

a transfer system configured for transferring the substrate within the processing tool;

at least one processing system configured for performing a trimming process on the gate electrode structure to form a trimmed dimension;

at least one controller configured for storing a process model capable of creating a set of process parameters from the first dimension and a target trimmed dimension, and controlling the set of process parameters in the trimming process; and

a further processing system for measuring the first dimension, the trimmed dimension of the gate electrode structure or both.

35. The processing tool according to claim 34, wherein the at least one processing system is configured to repeat the performing at least once until the target trimmed dimension is obtained.

36. The processing tool according to claim 35, wherein the further processing system measures the trimmed dimension and feeds the trimmed dimension back to the at least one controller to create a new set of process parameters.

37. The processing tool according to claim 34, wherein the at least one controller:

calculates a reaction layer thickness from at least one of the first dimension, the trimmed dimension, and the target trimmed dimension; and

determines the set of process parameters based on the reaction layer thickness.

38. The processing tool according to claim 37, wherein the at least one controller determines the set of process parameters by selecting at least one process parameter while keeping other process parameters fixed.

39. The processing tool according to claim 34, wherein the set of process parameters comprises process gas pressure, substrate

temperature, plasma power, process time or a combination of two or more thereof.

40. The processing tool according to claim 34, wherein the further processing system comprises a scattering technique, a scanning electron microscope (SEM) or both.

41. The processing tool according to claim 34, wherein the at least one processing system:

forms a reaction layer through reaction with the gate electrode structure; and

selectively removes the reaction layer from the unreacted portion of the gate electrode structure by chemical etching.

42. The processing tool according to claim 41, wherein the reaction layer is formed in a self-limiting process.

43. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to a reactant gas in a thermal process, a plasma process or both to form the reaction layer.

44. The processing tool according to claim 43, wherein the reactant gas comprises an excited oxygen-containing gas.

45. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to a wet oxidation process to form the reaction layer.

46. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to an etch gas to remove the reaction layer.

47. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to $HF_{(aq)}$ to remove the reaction layer.

48. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to HF and NH_3 gases and then to a heat treatment.

49. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to NF_3 and NH_3 gases in a remote plasma and then to a heat treatment.

50. The processing tool according to claim 41, wherein the at least one processing system exposes the gate electrode structure to a wet process.

51. The processing tool according to claim 41, wherein the at least one processing system consists of a single processing system.

52. The processing tool according to claim 41, wherein the at least one processing system comprises multiple processing systems.

53. The processing tool according to claim 34, wherein the first dimension is a lithographic dimension.

54. The processing tool according to claim 41, wherein the at least one processing system forms an oxide layer on a surface of the gate electrode as the reaction layer.

55. The processing tool according to claim 34, wherein the gate electrode structure comprises a gate electrode layer.

56. The processing tool according to claim 55, wherein the gate electrode layer comprises a Si-containing layer, a metal-containing layer or both.

57. The processing tool according to claim 56, wherein the gate electrode layer includes the Si-containing layer comprising amorphous Si, poly-Si, or SiGe or a combination of two or more thereof.

58. The processing tool according to claim 56, wherein the gate electrode layer includes the metal-containing layer comprising a metal, a metal nitride, a metal oxide or a combination of two or more thereof.

59. The processing tool according to claim 58, wherein metal-containing layer comprises TaN, TiN, TaSiN, Ru, RuO_2 or a combination of two or more thereof.

60. The processing tool according to claim 55, wherein the gate electrode structure further comprises an ARC layer.

61. The processing tool according to claim 60, wherein the ARC layer comprises an organic ARC layer or an inorganic ARC layer.

62. The processing tool according to claim 60, wherein the ARC layer comprises SiN.

63. The processing tool according to claim 34, wherein the at least one processing system is configured for wet processing.

64. The processing tool according to claim 34, further comprising an additional processing system configured for plasma etching.

65. The processing tool according to claim 64, wherein the additional processing system is configured for RIE.